ABSTRACT OF THE DISCLOSURE

In a memory unit provided by the present invention, unit blocks are laid out to form a block matrix. Each of the unit blocks has a plurality of memory cells arranged to form a cell matrix and a redundant line including a redundant memory cell. A plurality of unit blocks in the block matrix forms a one-dimensional group oriented in a first or second direction so that unit blocks pertaining to each one-dimensional group share a redundant line. Self-repair means embedded in the same chip as the memory unit stores only a minimum number of address pairs required for determining a redundant line to be used for repairing an abnormal memory cell for each unit block in storage means. The address of the redundant line to be used for repairing an abnormal memory is then found for each unit block on the basis of the minimum number of address pairs stored in the storage means. By storing only minimum required address information as such, a small size of the storage means and, hence, small circuit scales are sufficient. In addition, since a repair search is carried out by the embedded self-repair means in the same chip as the memory unit, the repair search can be carried out at a high processing speed.